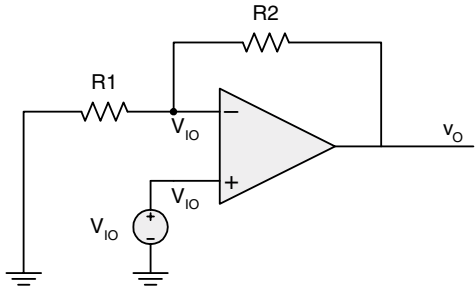

FIGURE 14.8 Analysis of input offset voltage.

the accuracy of the op-amp, the manufacturer will specify V_{IO} at room temperature (25°C) and at other temperature thresholds and provide coefficients or charts that relate the change in V_{IO} to temperature. Some op-amps, including the LM741, include compensation inputs that can be used to null-out the input offset error with external resistors. There is a limit to the practicality of this approach, however, resulting from temperature effects and the variation between components.

V_{IO} may not cause much trouble in an op-amp circuit with small gain, because a few millivolts of offset may be relatively insignificant as compared to several volts of actual signal. However, high-gain op-amp circuits that handle inputs with amplitudes in the millivolt range may be substantially degraded by V_{IO} effects. It may be desirable to AC-couple the op-amp's input when the frequencies of interest are high enough to make AC coupling feasible. The inverting circuit in Fig. 14.9 uses a capacitor to block a DC path to the op-amp's negative input. Because V_{IO} is a DC offset, the gain of the circuit is analyzed at DC to determine the amplification of V_{IO}. The impedance of the capacitor is ideally infinite at DC, resulting in unity gain for V_{IO}. For this circuit to function properly, the input frequency must be sufficiently high to not be attenuated by the highpass filter created by the series resistor and capacitor. The circuit exhibits a cutoff frequency where $f_C = 1 \div 2\pi C\text{R1}$. Therefore, frequencies much larger than f_C will be amplified by the idealized gain factor, –(R2 ÷ R1), when the capacitor essentially becomes a short circuit between the input and R1. The result is high gain at the frequencies of interest, yielding volts of output magnitude with only millivolts of V_{IO} error resulting from unity gain at DC.

Another parameter that relates to input offset voltage is the *power supply rejection ratio* (PSRR). The PSRR relates changes in the supply voltage to changes in V_{IO}. As the power rails fluctuate during normal operation, they influence the internal characteristics of the op-amp. PSRR is expressed in decibels as

$$PSRR = 20\log\frac{\Delta V_{CC}}{\Delta V_{IO}}$$

The LM741's minimum PSRR is specified at 77 dB. To ease arithmetic for the sake of discussion, we can round up to 80 dB and calculate PSRR = 10,000. This means that for every 1-V change in the supply voltage, V_{IO} changes by 100 μV. We know that V_{IO} is amplified by the gain of a DC-coupled circuit from the example in Fig. 14.8, indicating that a high-gain circuit is more susceptible to PSRR effects. PSRR declines with increasing frequency, making an op-amp more susceptible to power supply fluctuations.

Nonzero input currents are another source of inaccuracy in op-amp circuit, because real op-amps do not have infinite input resistance. Small nonzero currents flow into and out of the op-amp's in-

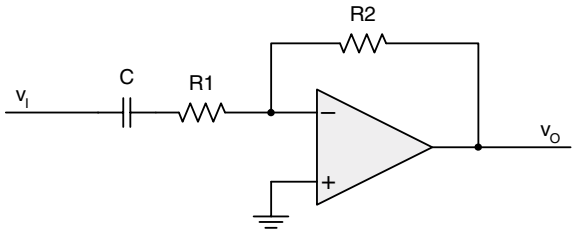

FIGURE 14.9 Mitigating V_{IO} with AC coupling.

puts. This current is the *input bias current*, I_{BIAS}. Ideal analyses of the preceding circuits assume that all currents flowing through R1 flow through R2 as well. This is clearly not true when the input impedance is finite. The result is that undesired voltage drops are created as input bias currents are drawn through resistors in an op-amp circuit. Consider the basic circuit in Fig. 14.10 with the inputs grounded to isolate I_{BIAS} effects independently from any input signal. The positive terminal remains at 0 V despite nonzero I_{BIAS}, because there is no resistance between it and ground (wire resistance is negligible). Therefore, the negative terminal is also at 0 V according to the virtual short assumption. While there is no current flowing through R1, because there is no voltage drop across it, I_{BIAS} flows from the output through R2. This results in a nonzero output voltage of $V_O = I_{BIAS}$R2 despite the fact that the circuit's inputs are grounded.

As seen in the LM741 data sheet, I_{BIAS} is measured in nanoamps for bipolar devices. CMOS op-amps specify I_{BIAS} in picoamps because of higher impedance MOSFET inputs. Practically speaking, many op-amp circuits with resistors measuring several kilohms or less do not have to worry about I_{BIAS} effects, because the product of nanoamps and resistance on the order of 10^3 Ω is on the order of microvolts. Of course, as circuit gains increase and allowable margins of error decrease, I_{BIAS} effects start to cause trouble. The problem is compounded by the fact that I_{BIAS} is not identical for each op-amp input as a result of slight physical variations in the circuitry associated with each input. A specification called *input offset current*, I_{IO}, is the difference between the two input bias currents. As seen in the LM741 data sheet, I_{IO} is smaller than I_{BIAS}, making I_{BIAS} the more troublesome characteristic.

Finite input bias current effects can be minimized by matching the induced offset voltages developed at each input. In Fig. 14.10, I_{BIAS} flowing into the positive terminal does not cause a voltage drop, which forces a corresponding I_{BIAS} to flow through R2 and create a nonzero output voltage. This circuit is augmented as shown in Fig. 14.11 by adding a resistor, R3, to the positive terminal.

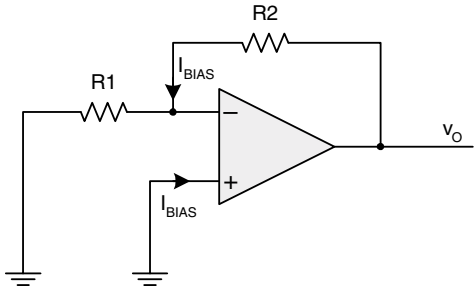

FIGURE 14.10 Analysis of input offset current.